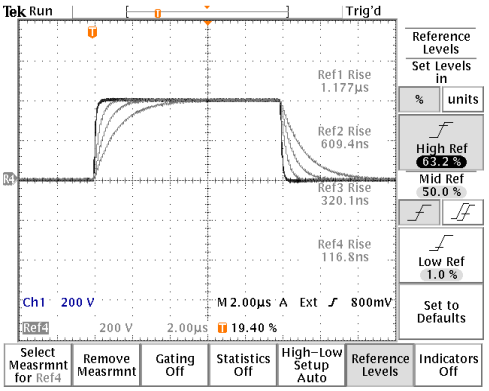
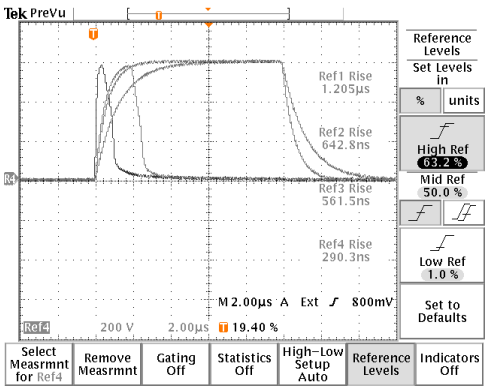
AVR-DV SERIES

PULSE GENERATORS
WITH ADJUSTABLE RISE TIMES
FOR PHOTOTRIAC dV/dt TESTS



+400V pulse across a Fairchild MOC3052M at different dV/dt. Even at the maximum dV/dt of 2164 V/us, no breakdown occurs.



+600V pulse across a Fairchild MOC3052M at different dV/dt. Breakdown starts around dV/dt = 590 V/us.

- Pulses up to +1000V or -1000V
- Adjustable rise times

- dV/dt to 2 kV/us at 400V
- Ideal for phototriac tests

Model AVR-DV1-B is a high performance, GPIB and RS232-equipped test system designed to produce waveforms suitable for phototriac dV/dt test requirements.

More specifically, the AVR-DV1-B mainframe generates a 500 ns to 200 us pulse with amplitude adjustable up to +1000V or -1000V. The rise and fall times of this pulse are < 100 ns. This pulse is applied to the supplied test fixture. An adjustable series resistance and a fixed capacitance are present in the test fixture. Together with the 50 Ohm output impedance in the mainframe, these generate a low-pass filter. The resulting 1%-63.2% rise time ("T") is < 125 ns to > 1.1 us, approximately.

By varying "T", different dV/dt rates can be obtained. Normally, the user will set the amplitude to a specific value, and increase the dV/dt value until the device under test (a phototriac) triggers, causing the voltage across the DUT to fall to zero.

The AVR-DV1-B model includes one AVX-DVDT-EVC test jig. The instrument mainframe is connected to the test jig using one coaxial cable and one DB-9 control cable. The test jig contains a ZIF socket suitable for a 6 pin DIP. The test jig has a hinged lid, which must be fully closed to protect the user from high voltages. The output will be automatically disabled if the lid is left open.

The AVR-DV1-B must be used in conjunction with a high-voltage oscilloscope probe (preferably with a BNC input connector) and an oscilloscope.

The AVR-DV1-B includes an internal trigger source, but it can also be triggered or gated by an external source. A front-panel pushbutton can also be used to trigger the instrument.

The AVR-DV1-B features front panel keyboard and adjust knob control of the output pulse parameters along with a four line by 40-character backlit LCD display of the output amplitude, pulse repetition frequency, and delay. The instrument includes memory to store up to four complete instrument setups. The operator may use the front panel or the computer interface to store a complete "snapshot" of all key instrument settings, and recall this setup at a later time.

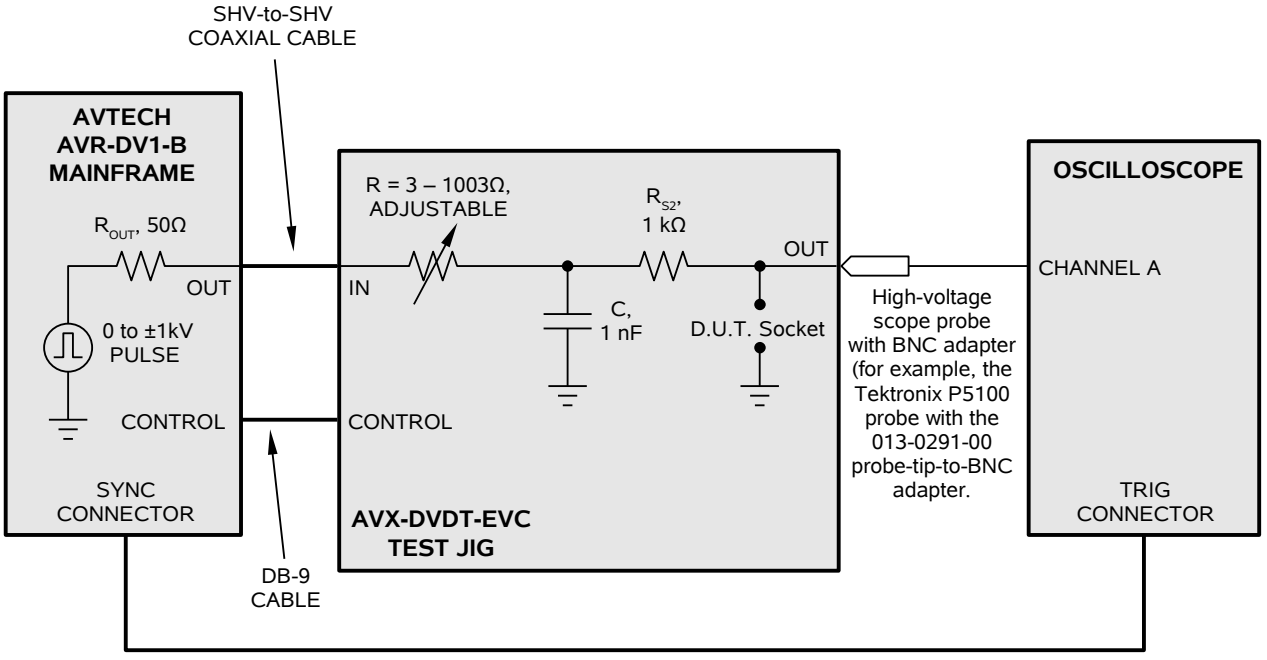
The "T" rise time is controlled by a mechanical potentiometer. It is not remotely-controllable.

Contact Avtech (info@avtechpulse.com) with your special test requirements!

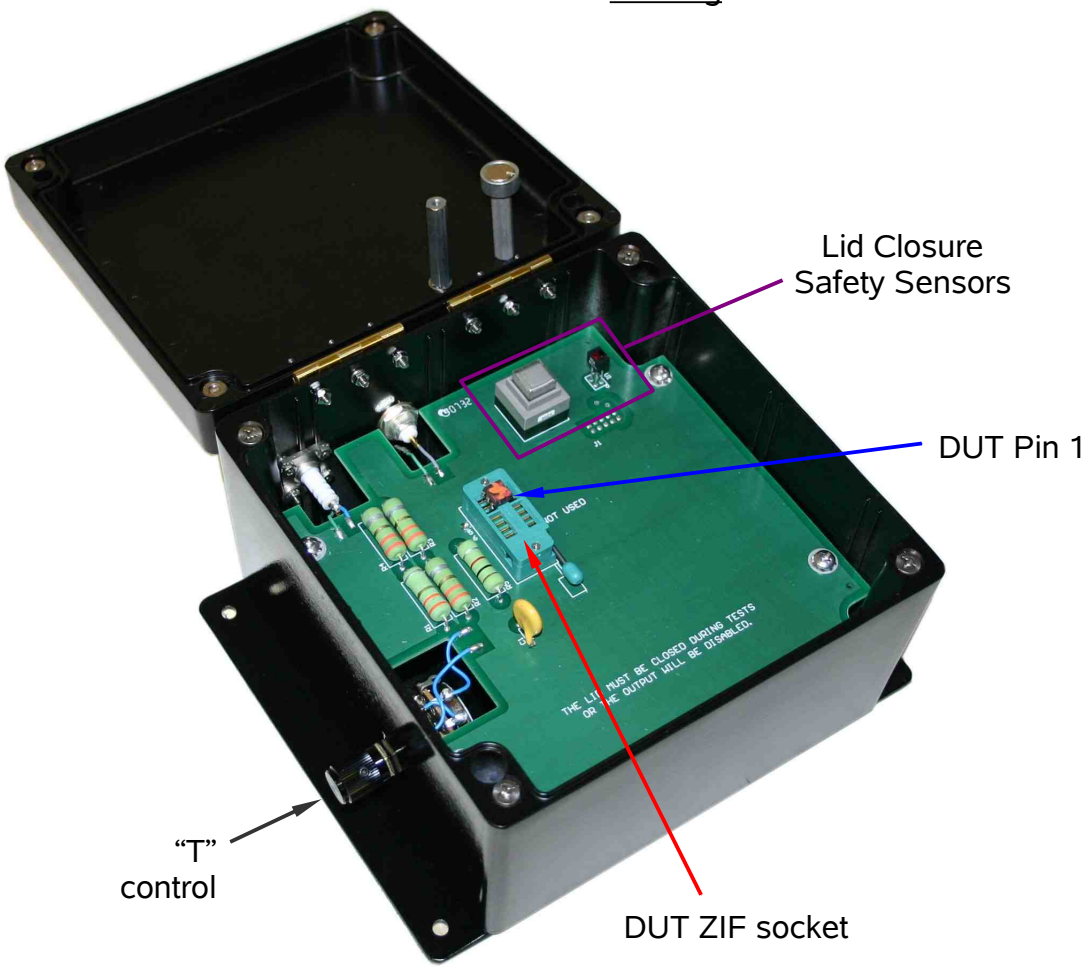
AVR-DV1-B Mainframe

Model[1]:	AVR-DV1-B
Amplitude: ($R_L \geq 50\Omega$) :	0 to 1000 Volts
Output impedance:	50 Ohms (at mainframe output)
Rise & fall times (20%-80%):	≤ 100 ns (at mainframe output)
Rise & fall times (1%-63.2%):	T = ≤ 125 ns to ≥ 1.1 us (measured across the DUT, in the test jig)
Pulse width (FWHM)[2]:	500 ns to 200 us
Maximum PRF:	400 Hz
Duty cycle (max):	0.02%
Max. droop at max. pulse width:	6%
Polarity:	+ or -, switchable
GPIB and RS-232 control[1]:	Standard on -B units. See http://www.avtechpulse.com/gpib for more information.
LabView Drivers:	Available at http://www.avtechpulse.com/labview. Note that "T" can not be remotely adjusted. It is adjusted using a mechanical potentiometer.
Internet control (Telnet & Web):	Optional[3]. See http://www.avtechpulse.com/options/tnt for details.
Propagation delay:	≤ 200 ns (Ext trig in to pulse out)
Jitter (Ext trig in to pulse out):	± 100 ps ± 0.03% of sync delay
Trigger required, Ext Trig mode:	Mode A: +5 Volt, 50 ns or wider (TTL) Mode B: +5 Volt, $PW_{IN} = PW_{OUT}$ (TTL)
Sync delay:	Variable 0 to ± 100 us (sync out to pulse out)
Sync output:	+3 Volts, 100 ns, will drive 50 Ohm loads
Gated operation:	Synchronous or asynchronous, active high or low, switchable. Suppresses triggering when active.
Connectors, Mainframe:	OUT: SHV. Trig, Sync, Gate: BNC
Test jig:	The test jig connects to the mainframe with a coaxial cable and a DB9 control cable (both are included). The test jig has a hinged lid. The mainframe output is disabled when the load is open. Tests must be performed with the lid closed. The jig contains a single ZIF socket suitable for a 6-pin DIP package (Anode = pin 1, Cathode = pin 2, Out = pin 6, Ground = pin 4, NC = pins 3 and 5). The clearance above the socket is > 2.5 cm (to accommodate package adapter usage).
Power requirements:	100 - 240 Volts, 50 - 60 Hz
Dimensions (H x W x D):	100 mm x 430 mm x 375 mm (3.9" x 17" x 14.8")
Chassis material:	cast aluminum frame and handles, blue vinyl on aluminum cover plates
Mounting:	Any
Temperature range:	+5°C to +40°C

1) -B suffix indicates GPIB-equipped model.
2) The output pulse width may also be controlled externally by applying a TTL-level trigger of the desired width to a rear-panel BNC connector ($PW_{IN} = PW_{OUT}$ mode).
3) Add the suffix -TNT to the model number to specify the internet control option.



Test Jig



The above photo also shows the location of the "T" control. This adjust the variable resistance "R", thus controlling the rise and fall times. In other words, it controls the "dt" portion of the key dV/dt ratio.

The IN, OUT, and CONTROL connectors are on the rear of the jig, below the hinges: